Contents

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1.1 License types/products

Product	License type	Board including xc2s50 FPGA	Board including xc2s100 FPGA	PC interface cable	Manual	Board schematic and library	Application software including source code# and compiled DLL	DLL source code#	Demo FPGA source code#	Download cable emulation FPGA source code#	CPLD Jedec file	CPLD source code#	Demo C code for 8051 CPU, utilities	registered users only	approx. Price €	Description
dlk51-n	N	-	-	-	x	x	x	-	x	-	x	-	x	-	free	basic package, non-profit
dlk51-nx	N	-	-	-	-	-	-	x	-	x	-	x	-	x	free	extra sources, non-profit
dlk51-50	N	1	-	1	x	x	x	-	x	-	x	-	x	-	298,00	board + basic package
dlk51-100	N	-	1	1	x	x	x	-	x	-	x	-	x	-	325,00	board + basic package
dlk51-50-edu	N	10	-	10	x	x	x	-	x	-	x	-	x	-	1900,00	education package
dlk51-100-edu	N	-	10	10	x	x	x	-	x	-	x	-	x	-	2100,00	education package
dlk51-p	P	-	-	-	x	x	x	x	x	x	x	x	x	x	498,00	full package, profit
dlk51-pm	-	-	-	-	x	x	x	x	x	x	x	x	x	x	298,00	1 year update renewal
dlkxx-t	-	-	-	-	-	-	-	-	-	-	-	-	-	-	45,00	development-time, 60 minutes*

source code, delivered sources. Limitations depending on license type, see down

** (Purpose: buying development time or building application specific blocks.)*

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2 Extent of delivery

For products dlk51-50 and dlk51-100:
- hardware ´dlk51´
- CD-ROM containing software ´dlk51´, manual in PDF format, schematic in EAGLE format, applications including source code for FPGA and 8051
- PC interface cable, D25male/D25female, 1:1
- optional: wall plug-in power supply

For other products see table 1.1, license types/products.

3 First steps

Thank You for using one of our products. Additional information may be available at **http://www.seng.de** .

3.1 Safety, electromagnetic compatibility (EMC)

This product is specified for use as **test and prototype platform for hardware and software development in laboratory environments** or for **installation in electrical appliances**. Hard- and software programmed into this product, as well as product environment, has strong influence on safety- and EMC-behaviour. Use, processing and operation of this product must be limited to trained persons or institutions and be in accordance to legal provisions, safety- and EMC-rules. This product is sensitive to ESD, handle only at static-safe workstations.

3.2 System requirements

- x86 based personal computer with one parallel printer port and and one CD drive
- Windows 9x/NT 4.0 based operating system

3.3 Installation

- read license terms, see chapter 1. Complete and return registration card
- insert dlk51 CD
- open Windows Explorer
- select CD drive, select path **D:\SENG**, where D is the CD drive
- double click on "**setup.exe"** to run installation program
- follow instructions on screen
- **if product type is dlk51-100, see chapter 6.2 (run BATCH "SelectDlk51-100.bat")**
- read file "**readme.txt**" at **D:\SENG\Doc**, where D is the CD drive
- if dlk51 is used with eLAB2dlk51-adapter ("eLABbase"), see chapter 5.10 - remarks 4 and 5
- connect dlk51 board connector X1 via delivered D25male/D25female interface cable to PC parallel printer port
- connect dlk51 with power supply (8-12VDC/12V AC) → LED named ON should be on

Attention: The driver for hardware access is installed automatically when program "dlk51" is executed the first time. For driver installation/deinstallation system administrator privileges are necessary. Deinstallation of driver can only be done manually before program deinstallation by calling batch "UnHWAcc.bat". Parallel port settings via BIOS setup should be set to EPP, PS2, SPP or equivalent, see chapter 4.3.

3.4 Demonstration

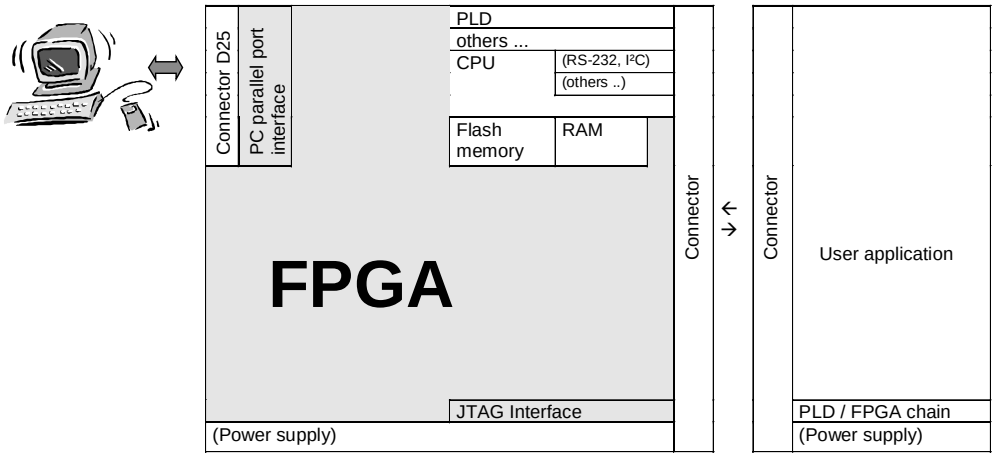
- double click on "dlk51" icon at Windows desktop. Hint: when program is executed the first time administrator privileges are necessary, see chapter 3.3.
- select **File → Setup → AutoSetup**
- select **FPGA → Config via PC → → FlashFastTestLed.bit**
- LED named TEST should flash fast
- select **FPGA → Config via PC → → FlashSlowTestLed.bit**

- LED named TEST should flash slow
- select **File → Exit**
- all LED´s should be off
- double click on dlk51 icon at Windows desktop
- last active configuration should be active again (FlashSlowTestLed.bit)
- LED named TEST should flash slow
- select **FPGA → Config via PC → → Demo1Fpga8032.bit**
- select **File → Program flash → CPU file3 → → FlashTestLed.bin**
- select **CPU → Run file3**
- LED named TEST should flash fast and slow
- select **Command → Commandline**
- enter **o 3 1**
- LED named TEST should flash 3 times with long time period off
- select **CPU → Disable**
- LED named TEST should be permanent on
- select **CPU → Run file3**
- LED named TEST should flash 3 times with long time period off
- play around (but read the manual ...),
- (select **Command → Commandline,** enter **o 3 2**, enter **o 3 3**, enter **o 3 0**, ...)

4 The dlk concept

The ´digital logic kernel´ is an easy to use technology to design, build and program logic blocks containing any kind of CPU with external program memory, programmable logic and flash memory. There is no need for any programming equipment or pre-programming of parts before use. The ´dlk´ is by default a self bootable device. It can be accessed via an integrated PC parallel printer port interface to exchange data or for administration purposes.
The only tool needed to build, program and service devices in the field is a state of the art PC with one parallel printer port. The ´dlk´ is implemented by use of Xilinx parts and design software.
Summary: ´digital logic kernel´= CPU+memory+FPGA+PCinterface = bootable system = ´ease of use´

The ´dlk´concept



4.1 Features

- build logic systems by using proven, reliable, expandable and easy to use kernels
- fast development cycles
- adaptable to any kind of CPU with external program memory
- consists of standard FPGA and CPLD parts, no special parts needed
- transfer data to and from those parts via the integrated parallel port interface
- internal bus master can be external PC or internal CPU
- parallel port interface to PC, can be used for data transfer and administration

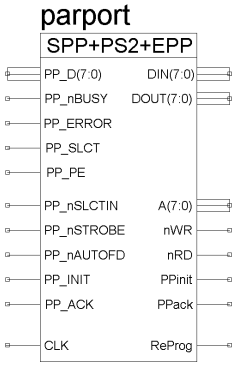
- parallel port interface reserves minimum amount of internal FPGA, if not used no internal resources are occupied
- administration software included
- software kernel included as DLL
- software and hardware kernel available as source code
- full featured implementation occupies just about 8% the slices of xc2s50 FPGA plus one xc9572xl CPLD
- upgradeable in the field
- build complete logic systems without the need of any kind of programming equipment hardware
- easy expandable design
- compatible to Xilinx ISE WebPACK
- emulation of Xilinx JTAG download cable (DLC5), compatible to iMPACT programming software
- Xilinx ISE WebPACK available for free
- use schematic entry, VHDL, Verilog or ABEL to enter a design

4.2 What for

- development platform
- implement logic kernels in any kind of user application
- build standard blocks for re-use in many applications
- for test purposes with need to be accessed by a PC via a standard interface
- as interface between an existing pice of hardware and a PC
- build systems with integrated PC interface
- build systems without expensive development tools
- for educational use
- cross development of controller based hardware on the PC
- rapid prototyping

4.3 PC parallel port interface

The interface enables a standard PC to communicate with an FPGA based peripheral device and to directly control it. The parallel port interface is completely realized as FPGA macro. The interface needs 51 slices of an xc2s-series FPGA, meaning it occupies about 7% the slices of an xc2s50 device (4% of an xc2s100). On the left hand side of the symbol are the PC parallel port signals, these pins have to be directly connected to FPGA I/O´s.



The clock pin has to be connected to the clock signal. On the right hand side is a 8-bit bus structure with seperate nWR and nRD signal, capable to directly address 256 addresses.

DIN(7:0)	data input bus
DOUT(7:0)	data output bus
A(7:0)	address output bus
nWR	data write strobe, active low
nRD	data read strobe, active low
PPint	additional output signal
PPack	additional input signal
ReProg	CfgPP register, ReProg bit

The macro itself consists of schematics and VHDL code realizing logic, registers, digital filters, synchronization and state machines. Driver software for Windows 9x/NT4.0 based operating systems is available in DLL format, setup to PC parallel port type and operating system is performed automatically.

Typical data transfer rates in Kbytes/sec:

PC parallel port type	EPP	PS2	SPP
outbyteS(), streaming	526	262	262
outbyte(), with addressing	255	134	134
inbyteS(), streaming	526	203	116
inbyte(), with addressing	250	116	81

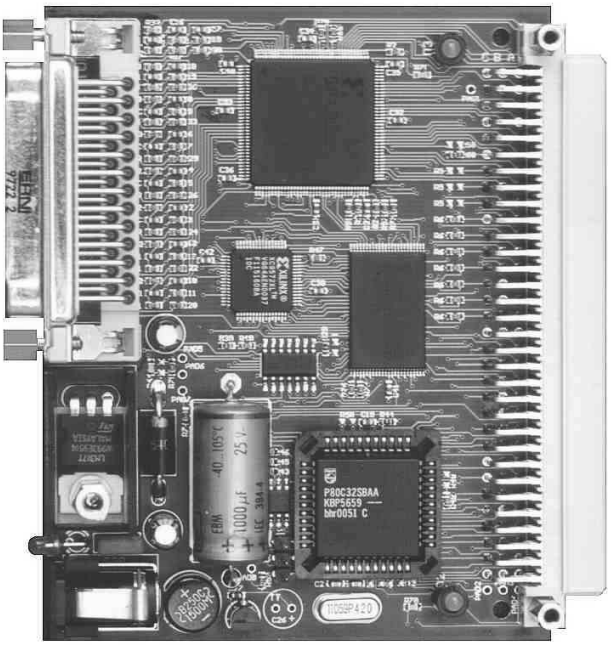
Parallel port settings via BIOS setup should be set to EPP, PS2, SPP or equivalent. For best performance settings should be set to EPP mode. Avoid to use settings like ECP or ECP/EPP, these may not offer full performance.

4.4 Implementations

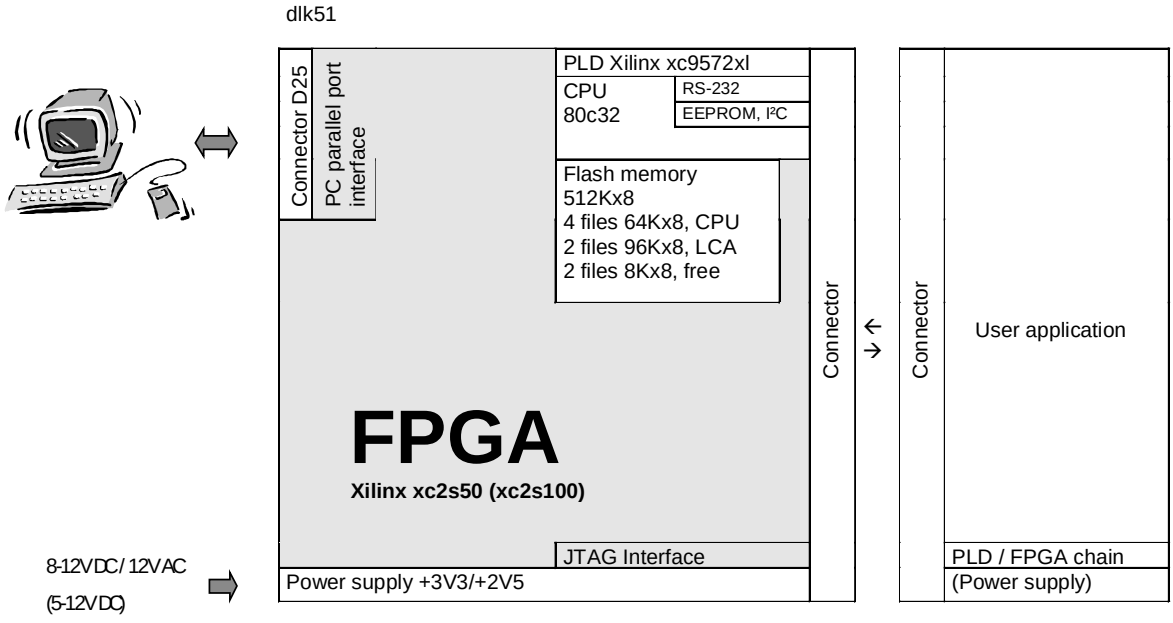
- dlk51, existing
- dlk32, planned, integrating 32-bit (soft-)CPU

5 Hardware

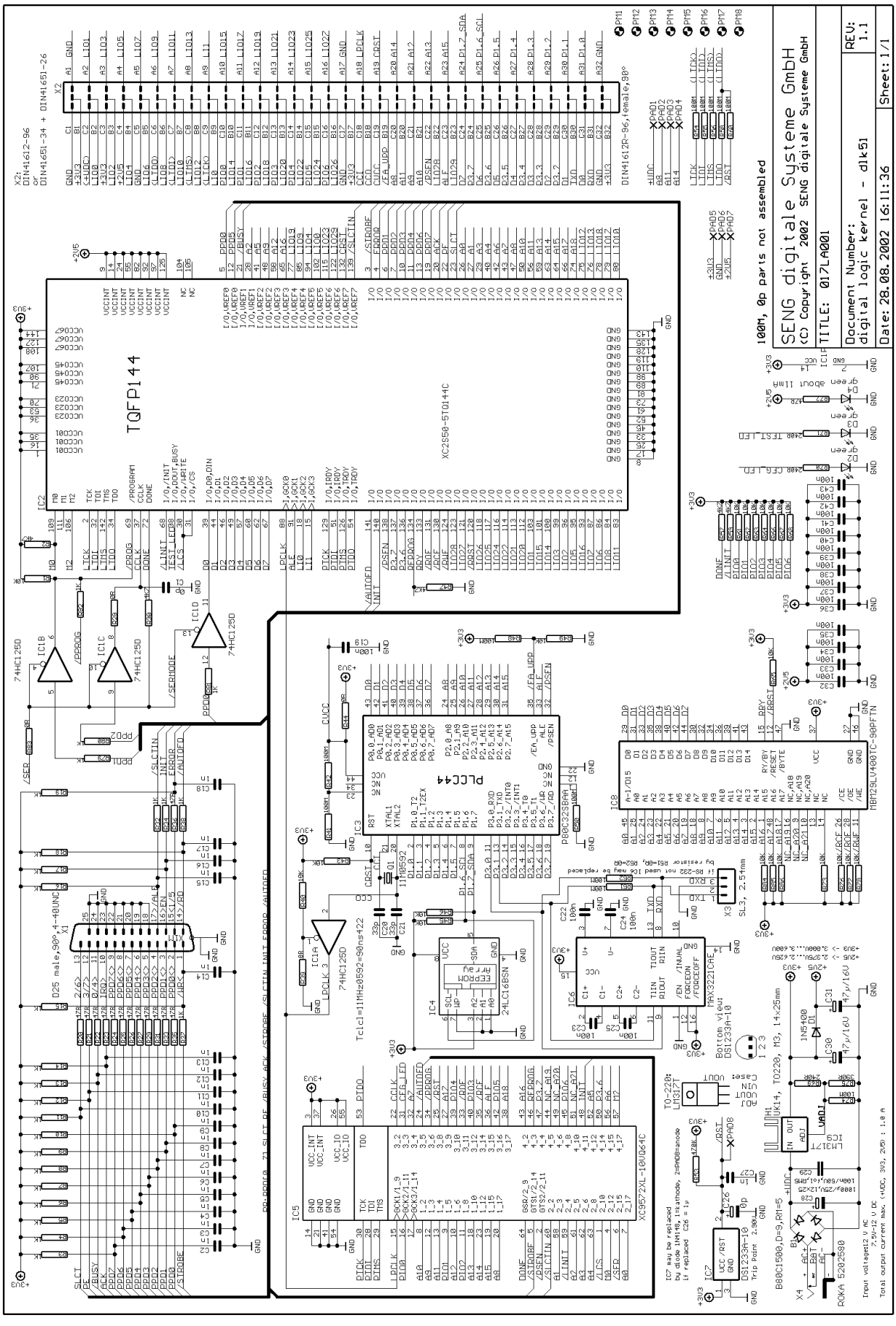
5.1 Overview



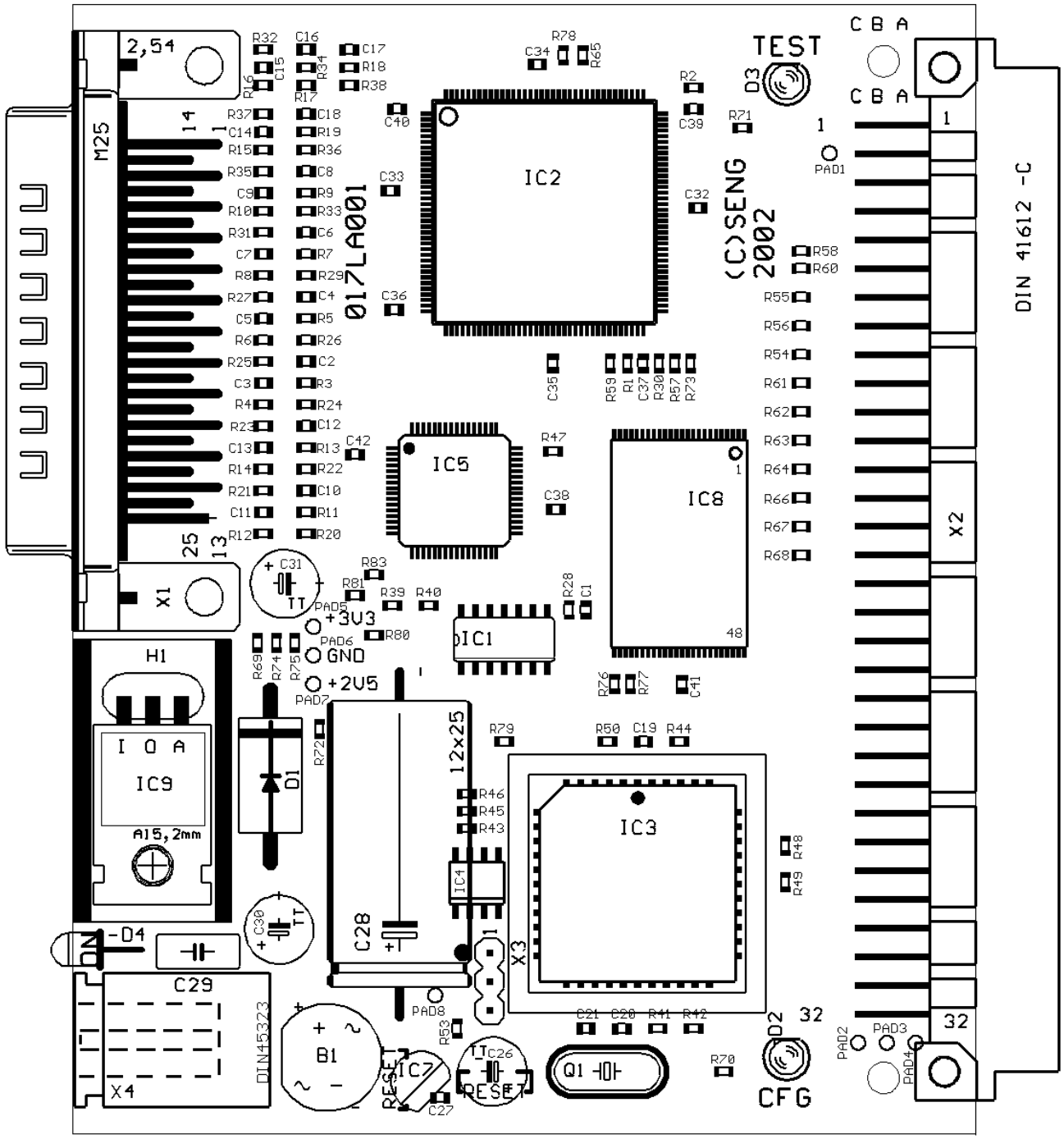
- FPGA xc2s50 (optional xc2s100)
- CPLD xc9572xl
- 8-bit 8032 CPU running at 11MHz0592
- serial RS-232 interface connected to CPU
- 16Kbit I²C EEprom connected to CPU
- CPU can be used in bus or I/O mode
- external CPU bus connected to FPGA
- single 512Kx8 flash memory for CPU and FPGA
- two LED´s for debug and display purposes
- reset monitor circuit for power failure detection and external reset
- all 3V3 design
- 2 independent FPGA configuration files in flash memory, selectable via jumper before boottime
- 4 independent 64Kx8 CPU program files in flash memory, selectable via ´dlk51´ software or FPGA setup
- PC or 8032 microcontroller can be used as host CPU for internal bus
- fast data transfer (500Kbytes/sec, typical) to/from PC via PC parallel printer port interface, connector D25 male
- linear power supply on board, input 8-12V DC/12V AC/1500mA (optional 5-12V DC/800mA), connector DIN45323
- all signals available at 96-pin connector DIN 41612
- user extension boards can be installed inline or as stack
- board size 80x100mm
- about 92% of internal xc2s50 FPGA resources (without PC interface 100%) + 32 I/O´s available to user
- Emulation modes for ATMEL AVR ISP DONGLE and XILINX JTAG download cable (DLC5 / Parallel Cable III)
- digital logic kernel for application, test, development and education



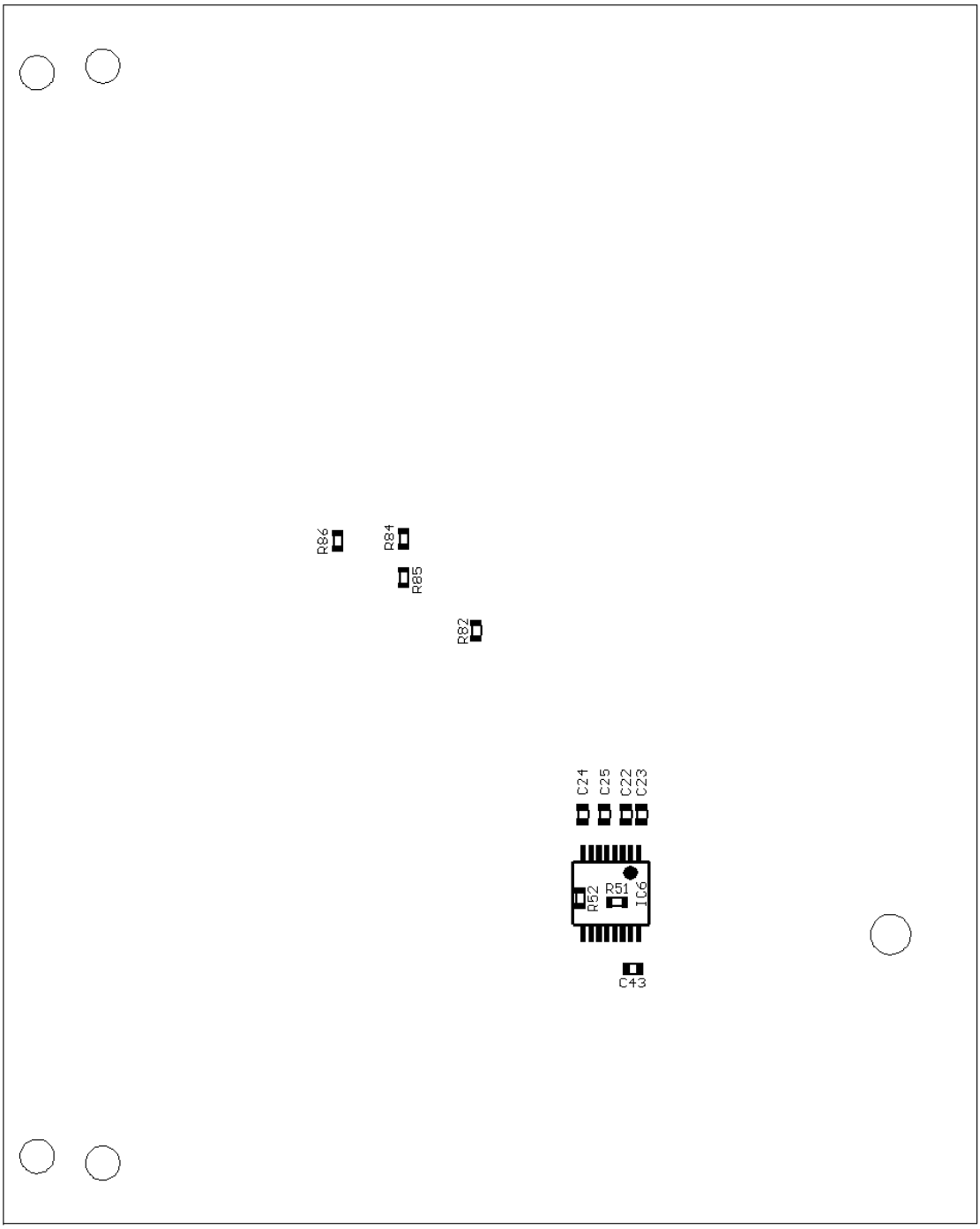
5.2 Schematic



5.3 PCB component side



5.4 PCB solder side



5.5 Partlist

Qty	Value	Package	Parts
4	0R	R0603	R28, R39, R44, R83
~~1~~	~~0p~~	~~C0603~~	~~C1~~
~~1~~	~~0p~~	~~TT2D6~~	~~C26~~
25	1K	R0603	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R32, R34, R37, R38, R79, R80, R81, R82
1	1N5400	DO201-15	D1
18	1n, X7R	C0603	C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C27
5	4K7	R0603	R2, R30, R47, R57, R59
21	10K	R0603	R1, R40, R43, R45, R46, R49, R61, R62, R63, R64, R65, R66, R67, R68, R73, R76, R77, R78, R84, R85, R86
1	11M0592	HC49/S	Q1
1	24LC16BSN	SO-08	IC4
2	33p, NP0	C0603	C20, C21
2	47µ/16V	TT2D6	C30, C31
14	47R	R0603	R20, R21, R22, R23, R24, R25, R26, R27, R29, R31, R33, R35, R36, R72
1	74HC125D	SO14	IC1
~~12~~	~~100M~~	~~R0603~~	~~R41, R42, R48, R50, R51, R52, R54, R55, R56, R58, R60, R74~~
17	100n, Z5U	C0603	C19, C22, C23, C24, C25, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43
1	100n/50V,fol,RM5	C050-030X075	C29
3	240R	R0603	R69, R70, R71
1	390R	R0603	R75
1	470K	R0603	R53
1	1000µ/25V,12x25	E30-12, axial	C28
1	B80C1500,D=9,RM=5	RB1A	B1
1	D25 male,90°,4-40UNC	M25HP	X1
1	DIN41612R-96,female,90°	MABC96L	X2
1	DS1233A-10	TO92	IC7
1	LM317T	317TL	IC9
1	MAX3221CAE	SSOP16	IC6
1	MBM29LV400TC-90PFTN	TSOP48	IC8
1	P80C32X2BA or P80C32SBAA	PLCC-44_2	IC3
1	ROKA 5202580	DIN45323_ROKA	X4
1	SL3, 2.54mm	MA03-1	X3
1	UK14, TO220, M3, 14x25mm	UK14SAM3	H1
1	XC2S50-5TQ144C	TQFP-144	IC2
1	XC9572XL-10VQ64C	VQFP64	IC5
3	green	LED3MM	D2, D3, D4
1	PLCC44-Socket SMD		IC3
2	LED Halter 3mm/L=4.5mm	Bü 32G2750	D2,D3
2	Stehbolzen, 4-40UNC, L=5mm		X1
1	Schraube M3x12,Torx	Fa 250-119	H1
1	Abstandsbolzen M3x12.5	Bü 18H2466	IC9
1	Isolierscheibe M3	TO-220/1mm	IC9
1	Isolierscheibe TO-220	Bü 61B646	IC9,selbstklebend
~~4~~	~~PASSMARK~~	~~PASSMARK~~	~~PM1, PM2, PM3, PM4~~
~~5~~	~~PASSMARKS~~	~~PASSMARKS~~	~~PM5, PM6, PM7, PM8, PM9~~
1	Leiterplatte 017LA001		
1	Datenkabel D25, 2m/1:1	male/female	Zubehör
1	CD incl. copy		Zubehör
2	Schraube M2.5x12/DIN7985		X2
2	Mutter M2.5		X2
2	Unterlegscheibe M2.5x0.5	Kunststoff	X2

5.6 LED´s

ON, D4: on if power supply active.

CFG, D2: on if FPGA is configured.

TEST, D3: on/off under control of FPGA and/or CPU.

5.7 Power supply, connector X4

Connector type DIN 45323, ground at center pin

Input voltage 8...12VDC / 12V AC
Input current limited by linear voltage regulator and heatsink capability, max 1.5A.

Output voltage +UDC (not regulated), 3V3, 2V5.
Total output current (+UDC, 3V3, 2V5) max. 1.5A.

Heatsink capability, type UK14: 20K/W → Maximum power loss (∆T=70K): 70/20 = 3.5W
→ Max. total output current without additional heatsink (8VDC input voltage): 3.5 / 8-(2+3.3)) = 1.3A
→ Max. total output current without additional heatsink (12VDC input voltage): 3.5 / (12-(2+3.3)) = 0.5A
Higher total output currents can be achieved by using additional heatsink.

+UDC can be made available at user port connector X2, by connecting PAD1 with pin C2 of connector X2 via a solder joint at solder sider of PCB. If connected pay attention of high voltage (6..12VDC) and risk of unlimited current at user port connector. Can be used for generating additional voltages, for powering LCD backlight ...

5.8 Parallel port, connector X1

Connector type D25 male.
Connect to IBM-PC parallel printer port via delivered 1:1 interface cable. Port for administration, setup and data transfer purposes.
Function depending on software and FPGA configuration.
Attention: no isolation to PC printer port, all signals directly connected.

5.9 RS-232 port, connector X3

Connector type pin header 3 x 2.54mm.
Connected via RS-232 tranceiver to UART of CPU, see "schematic".

Pin	Signal
1	TXD
2	GND
3	RXD

If X3 is connected to IBM-PC RS-232 serial port following wiring is necessary:

IBM-PC D9 male, pin(signal)	X3, pin(signal)
1(DCD)-4(DTR)-6(DSR)	-
2(RXD)	1(TXD)
3(TXD)	3(RXD)
5(GND)	2(GND)
7(RTS)-8(CTS)	-
9(RI)	-

5.10 User port, connector X2 / FPGA pin assignments

DIN41612-96 or DIN41651-34+DIN41651-26* (bus connector **or** I/O port connector can be assembled)
peripheral chip select
°CPU signal connected to FPGA
^ RS-232 tranceiver may be installed on board
[2] select FPGA configuration boot file: high or open → file0 (default), low → file1
[3] depending on configuration this pin may be used for JTAG or ISP download cable emulation
[4] see chapter 5.7. Set solder joint for use with eLAB2dlk51-adapter. Default: +UDC not available
[5] depending on CPLD configuration file, not used (default) or charge pump driver (for eLAB2dlk51-adapter), see down

			eLAB base	FPGA Pin		eLAB base	FPGA Pin	
								DIN41651-34
DIN 41612-C	**C**	**B**			**A**			
1	GND	+3V3			GND			**2**
2	(+UDC)[4]	LIO0	P1	102	LIO1	P2	103	**4**
3	+3V3	LIO2	P3	96	LIO3	P4	99	**6**
4	+2V5	LIO4[3]	P5	94	LIO5[3]	P6	95	**8**
5	GND	LIO6[3]	P7	86	LIO7[3]	P8	87	**10**
6	(LTDO) (/RST)	LIO8	P9	84	LIO9	P10	85	**12**
7	(LTDI)	LIO10	P11	80	LIO11	P12	83	**14**
8	(LTMS)	LIO12	P13	75	LIO13	P14	76	**16**
9	(LTCK)	LI0	P31	18	LI1	P32	15	**18**
10	PIO0	LIO14	P15	100	LIO15	P16	101	**20**
11	PIO1	LIO16	P17	93	LIO17	P18	79	**22**
12	PIO2	LIO18	P19	78	LIO19	P20	77	**24**
13	PIO3	LIO20	P21	112	LIO21	P22	113	**26**
14	PIO4[5]	LIO22	P23	114	LIO23	P24	115	**28**
15	PIO5, EnLCD[#]	LIO24	P25	116	LIO25	P26	117	**30**
16	PIO6, SelFile[2]	LIO26	P27	118	LIO27	P28	121	**32**
17	GND	+3V3			GND			**34**
18	CCI	CCO			LPCLK			
19	CVCC	/EA_VPP			CRST°			
20	A8°	A11°			A14°			
21	A9°	A10°			A12°			**2**
22	/PSEN°	LIO28	P29	123	A13°			**4**
23	ALE°	LIO29	P30	122	A15°			**6**
24	D7°	P3.7_/RD°			P1.7_SDA			**8**
25	D6°	P3.6_/WR°			P1.6_SCL			**10**
26	D5°	P3.5_T1			P1.5			**12**
27	D4°	P3.4_T0			P1.4			**14**
28	D3°	P3.3_INT1			P1.3			**16**
29	D2°	P3.2_/INT0			P1.2			**18**
30	D1°	P3.1_TXD^			P1.1_T2EX			**20**
31	D0°	P3.0_RXD^			P1.0_T2			**22**
32	GND	+3V3			GND			**24**
	A8°	A11°			A14°			**26**
	bus connector*							**DIN41651-26***
		I/O port connector*						

User port pins, functionality and limitations:

Pin	Function
LIO4, LIO5, LIO6, LIO7	these signals may be used for JTAG or ISP download cable emulation
PIO4	"P017a002.JED" (default) → not used, "P017a004.JED" (eLAB2dlk51) → charge pump driver
PIO5, EnLCD	Chip select for optional "KS0070B" kompatible LCD display connected to CPU
PIO6, SelFile	select FPGA configuration boot file: high or open → file0 (default), low → file1
P1.6_SCL, P1.7_SDA	CPU pins used for i2c peripheral bus
P3.0_RXD, P3.1_TXD	CPU pins used for RS-232 serial port
CPU, all	see device data sheet and schematic
FPGA, all	see device data sheet and schematic
CPLD, all	see device data sheet and schematic

5.11 Pushbutton reset

optional pushbutton reset switch may be connected to pins on PCB named "RESET".
Functionality of DS1233A: A precision temperature-compensated reference and comparator circuit are used to monitor the status of the power supply (+3V3). When an out-of-tolerance condition is detected, an internal power failsignal is generated which forces reset to the active state. When VCC returns to an in-tolerance condition,the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233A is pushbutton reset control. The DS1233A debounces a pushbutton closure. Connecting signal /RST to GND will generate a 350 ms reset pulse upon release, see "schematic" for signals.

5.12 Bytewide Flash ROM memory assignment

FLASH-ROM memory used to hold setup data, FPGA configuration and CPU program memory files.

Size KByte	K-address	HEX-address	Memory use	Flash Sector Address
16	496-512	7C000h-7FFFFh	reserved for manufacturer use	SA10
8	488-496	7A000h-7BFFFh	not used	SA9
8	480-488	78000h-79FFFh	not used	SA8
64+32	384-480	60000h-77FFFh	FPGA configuration file1	SA6, SA7
64+64	256-384	40000h-5FFFFh	FPGA configuration file0 (default)	SA4, SA5
64	192-256	30000h-3FFFFh	CPU program file3	SA3
64	128-192	20000h-2FFFFh	CPU program file2	SA2
64	64-128	10000h-1FFFFh	CPU program file1	SA1
64	0-64	00000h-0FFFFh	CPU program file0 (default)	SA0

5.13 Connecting LCD display

Character LCD display module can be directly connected. Display must be compatible to 3V3 logic and power supply. Voltage Vo must be generated externally and adjusted to best contrast settings, otherwise content may not be visible. Table shown for: "Displaytech 162C-BC-BC" (16 characters x 2 lines, 80x36mm, "KS0070B" compatible display controller).

LCD 162C-BC-BC	LCD signal	dlk51
1	GND	GND
2	VCC	+3V3
3	Vo	(LCD input voltage, contrast setting, depending on display, -1V9...+3V3. Hint: for generating negative voltage use charge pump, see chapter 5.10 - remark 5)
4	RS	A9
5	R/W	A8
6	E	PIO5, EnLCD
7	D0	D0
8	D1	D1
9	D2	D2
10	D3	D3
11	D4	D4
12	D5	D5
13	D6	D6
14	D7	D7
15	BLA	(backlight LED anode, depending on display, Hint: see display datasheet for minimum voltage, almost always >> +3V3)
16	BLK	(backlight LED kathode, depending on display, Hint: almost always connected to GND)

Software C routines controlling LCD display, see chapter 8.2.2

6 FPGA Configuration

SRAM based FPGA circuits like the xc2s50 or xc2s100 used on this board need to be configured after power up before any operation is possible. This can be done on several ways. This board supports 2 of them:

- configure the FPGA via a serial data stream, realized by use of an external PC and it´s parallel port interface.
- configure the FPGA via a parallel data steam, realized by use of on board state machine and flash-memory.

Configuration data needs to be generated within a specialized design environment. One of these is Xilinx ISE. This design environment consists of entry tools like schematic editor, VHDL and state machine diagram entry, testbench generator, simulation tools, compilers, partitioning tools and others. This environment enables the user to define personalized logic the way he wants to. At the end of a successful logic implementation there will be a single configuration file holding all the information the FPGA needs for functioning.

6.1 Creating a configuration file

detailed description see Xilinx ISE manuals.When using Xilinx ISE default values for bitstream generation should be fine, the resulting bitstream file will be of type "ProjektName.bit". This file can be directly used for downloading or flashing with administration software "dlk51.exe".
Attention: special consideration should be kept to "pin locking", which means assigning I/O pins to FPGA I/O ressources. **Every FPGA or CPLD I/O pin used in a design (on a existing PCB board) has to be manually assigned (constrained) to a location, according to the needs of this already existing PCB board.** Always be aware of the board schematic and it´s already existing nets (never connect 2 or more enabled output pins).
DISREGARDING THIS NEEDS WILL PRODUCE SEVERE DAMAGE TO THE BOARD.

6.2 Existing FPGA designs

The dlk51 board is availabe in 2 different versions one equiped with an xc2s50 the other with an xc2s100 FPGA. Cause FPGA´s differ in gatecount the configuring bitstream files differ in size and content. Logic definition and pin assignment are not attached.

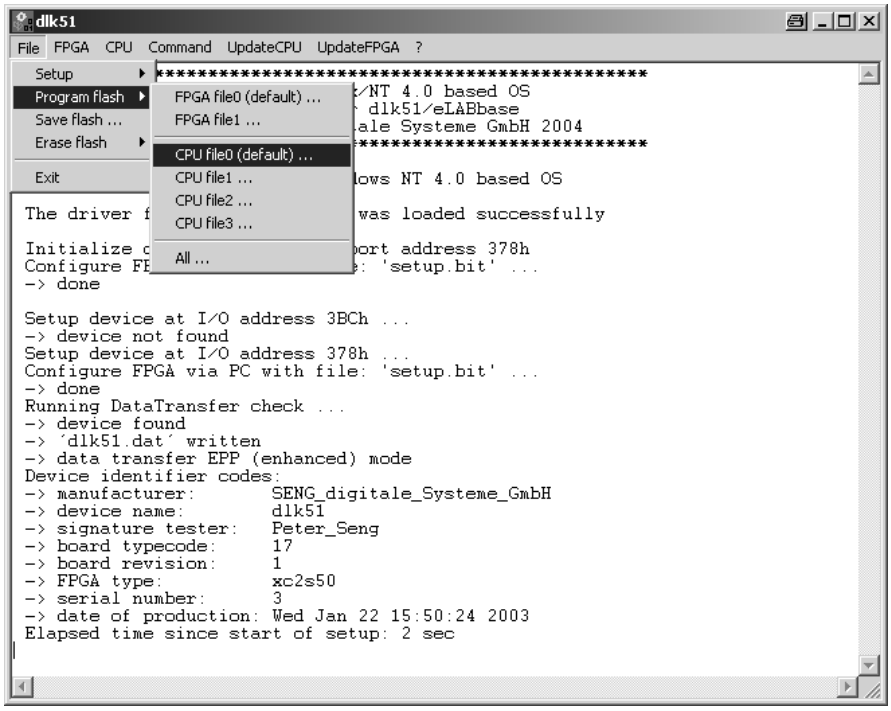
Product	FPGA Type	Filesize bitstream	User I/O	Logic cells	CLB´s	Slices	FF,LUT	Block RAM bits
dlk51-50	xc2s50	69 Kbytes	92	1728	384	768	1536	32K
dlk51-100	xc2s100	96 Kbytes	92	2700	600	1200	2400	40K

Existing FPGA designs delivered on CD are for dlk51-50 unless otherwise mentioned. Bitstream files are supplied for both types of FPGA (files for xc2s100 are named "xxxx.100_bit", where xxxx is the filename). If product type is dlk51-100 bitstream files have to be renamed to "*.bit". Use BATCH "SelectDlk51-100.bat" for doing this. If switching back to product type dlk51-50 is necessary use BATCH "SelectDlk51-50.bat". BATCH is located in the same directory where "*.bit" and "*.100_bit" files are. For configuring FPGA´s always use the corresponding file. If existing designs are re-compiled be aware of setting the device type to the FPGA type mounted on the board. Bitstream files of existing FPGA designs are automatically installed when administration program "dlk51.exe" is installed. Source files for Xilinx ISE are available on CD, see chapter 9.2. For extra sources (see chapter 1.1), see chapter 7. All files generated with XILINX ISE

Name	Functionality
Demo1Fpga8032.bit	PC parallel port interface and 8032-peripherals including latch, reset logic and file select logic
Demo2Fpga8032.bit	PC parallel port interface and extended 8032-peripherals including latch, reset logic, file select logic, 4 Kbytes RAM and i2c interface
eLABbaseTestA.bit	used for functional test of eLABbase I/O´s with external test-connector
eLABbaseTestB.bit	used for functional test of eLABbase I/O´s with external test-connector
emu*.bit	several files used for JTAG or ISP download cable emulations, external available at LIO4..LIO7
flashfasttestled.bit	demo, flash LED TEST fast
flashslowtestled.bit	demo, flash LED TEST slow
intdlc5.bit	used for emulating XILINX DLC5 JTAG download cable (program internal xc9572xl CPLD)
liotesta.bit	used for functional test of FPGA I/O´s with external test-connector
liotestb.bit	used for functional test of FPGA I/O´s with external test-connector
setup.bit	used for setup device and administration

7 Software dlk51

System requirements, installation and demonstration see chapter 3.



Development environment, software for administration, setup, test and data transfer. It consists of two parts. The program itself and a DLL containing the kernel functions. Extra sources (see chapter 1.1) are not delivered on CD. These are distributed on request via eMail, (registered users only), request form see internet pages, download area. All files generated with Microsoft Visual C++ 5.0.

The program is intended to be used as is and to be starting point of "dlk" based development projects. The delivered sources and functions allow rapid development of "dlk" based applications, test and development systems. Source files for "dlk51.exe" are available on CD, see chapter 9.2. An easy and powerfull way to **improve functionality** of "dlk51.exe" is adding new commands and functions to the commandline, see module "TestDlg.cpp", "CTestDlg::ExecuteCmdLine".

7.1 Functional overview

Command	Description
File → Setup → Autosetup	initialize board and data-transfer, search on all PC parallel printer ports
File → Setup → At port 3BCh	initialize board and data-transfer, search on PC parallel printer port 3BCh only
File → Setup → At port 378h	initialize board and data-transfer, search on PC parallel printer port 378h only
File → Setup → At port 278h	initialize board and data-transfer, search on PC parallel printer port 278h only
File → Program flash → FPGA file0 (default)	program on board FPGA file0 with configuration bitstream data
File → Program flash → FPGA file1	program on board FPGA file1 with configuration bitstream data
File → Program flash → CPU file0 (default)	program on board CPU file0 with program code
File → Program flash → CPU file1	program on board CPU file1 with program code
File → Program flash → CPU file2	program on board CPU file2 with program code
File → Program flash → CPU file3	program on board CPU file3 with program code
File → Program flash → All	program all on board FPGA and CPU files with PC ROM mirror file
File → Save flash ...	save all on board FPGA and CPU files to PC ROM mirror file
File → Erase flash → Fpga file0 (default)	erase FPGA file0
File → Erase flash → Fpga file1	erase FPGA file1
File → Erase flash → CPU file0 (default)	erase CPU file0
File → Erase flash → CPU file1	erase CPU file1
File → Erase flash → CPU file2	erase CPU file2
File → Erase flash → CPU file3	erase CPU file3
File → Erase flash → All	erase all FPGA and CPU files
File → Exit	save existing setup and exit program

FPGA → Config via PC ...	configure FPGA via PC parallel port interface
FPGA → Config via flash	configure FPGA via on board FPGA file
FPGA → Clear	clear FPGA configuration data
CPU → Run file0 (default)	run CPU program file0 active "Demo1Fpga8032.bit" or "Demo2Fpga8032.bit" required
CPU → Run file1	run CPU program file1 active "Demo1Fpga8032.bit" or "Demo2Fpga8032.bit" required
CPU → Run file2	run CPU program file2 active "Demo1Fpga8032.bit" or "Demo2Fpga8032.bit" required
CPU → Run file3	run CPU program file3 active "Demo1Fpga8032.bit" or "Demo2Fpga8032.bit" required
CPU → Disable	keep CPU reset activated active "Demo1Fpga8032.bit" or "Demo2Fpga8032".bit required
Command → Emulate → AT89isp cable	emulate ATMEL AT89isp cable via FPGA
Command → Emulate → AVR ISP dongle	emulate ATMEL AVR ISP dongle via FPGA
Command → Emulate → DLC5 / Parallel Cable III	emulate XILINX JTAG download cable DLC5 / Parallel Cable III via FPGA
Command → Save BASIC RAM ...	save MCS BASIC-52 programm to PC active "Demo2Fpga8032.bit" required
Command → Test FPGA I/O	test FPGA I/O, external test-connector required
Command → Test eLABbase I/O	test eLABbase I/O, external test-connector required
Command → CheckTransferRate	check data transfer rate PC ←→ dlk51 and display
Command → Commandline ...	open commandline window, for test and development, basic I/O
UpdateCPU	re-program on board CPU fileX with program code, run CPU
UpdateFPGA	re-configure FPGA via PC parallel port interface
? → About dlk51 ...	show program information

8 Add-on software and manuals

8.1 XILINX

Xilinx, manufacturer of CPLD and FPGA used to realize "dlk51", provider of complete programmable logic solutions, including semiconductors, software and documentation

8.1.1 Software

XILINX ISE WebPack, integrated software environment for developping FPGA and CPLD based logic. May be included on seperate CD, otherwise it can be downloaded from the web at
http://www.support.xilinx.com/support/download.htm

8.1.2 Documents and more

For links to manuals, datasheets, tutorials and additional stuff please consult
http://www.seng.de/dlk_database.html, section "Xilinx FPGA links"

8.2 SDCC C compiler

SDCC is a freeware, retargettable, optimizing ANSI-C compiler by Sandeep Dutta designed for 8 bit microcontrollers including 8051 family CPU´s. The entire source code for the compiler is distributed under GPL. Compiler is available on CD, see chapter 9.2 or **http://sdcc.sourceforge.net**

8.2.1 Additional information

To build a working 8051 kernel FPGA has to be configured with file "Demo1Fpga8032.bit" or "Demo2Fpga8032.bit".
SDCC C compiler has to be handeled via a command line interface. Handling can be made comfortable by using specialized BATCH files. For editing C style projekts every C Compiler IDE containing a C editor is suitable. We prefer using Microsoft Visual C++ 5.0 environment for editing and handling C projects. After saving all files and switching to a command line window, a batch in this window can be started to compile the files generated inside the IDE and to perform a hex to binary file-conversion.
Another suitable solution is using Jens' File Editor or Programmers Notepad. Some tools, including Hex-file conversion utility, are available on CD, see chapter 9.2, for others see **http://www.seng.de/dlk_database.html**, section "Tools"

8.2.2 C demo program source code

Demo C source code including LCD display, UART and i2c control routines are available on CD, see chapter 9.2

8.3 MCS BASIC-52 interpreter

MCS BASIC-52 interpreter was developed by INTEL for the 8052-AH microcontroler in the early 80´s of last century. It´s size is only 8Kbyte and it fits into the internal read only memory (ROM) of this processor. People say INTEL placed this interpreter as freeware to the public domain (but who really knows ? - We could not find any information on INTEL website, so we do not distribute -). The interpreter will run on any 8052-AH compatible CPU and always requires at least 1K bytes of external RAM. It must be available at program memory location 0000h. We do not recommend using BASIC for development or educational use. The use of SDCC C compiler is much more comfortable, code is faster, smaller, C code can be easily distributed or re-compiled for another architecture or another project and there is a lot of C source code available on the web. Do not waste time learning or using BASIC. So there is still one interesting question: Why was MCS BASIC-52 implemented on dlk51 ? Just out of historical reasons, it´s a nice demo to show "dlk" capabilities and emulating such old stuff is interesting, reminding of the days when this kind of programming was state of the art ...
Interpreter and manual available on the web, for links please consult **http://www.seng.de/dlk_database.html**, section "8051 CPU"

8.3.1 Additional information

For MCS BASIC-52 compatibility mode FPGA has to be configured with file "Demo2Fpga8032.bit". Connect dlk RS-232 serial port to PC serial port. Run terminal program on PC (9600 Baud, 8, n, 1).
PROG, PROGx, FPROG, FPROGx and PGM commands will not work, cause there is no external EPROM memory. The BASIC program existing in RAM can be read out and stored on the PC in a file by use of command **Command → Save BASIC RAM ...** , see chapter 7.1. Therefore MCS BASIC-52 needs to be in the RAM mode, else use MCS BASIC-52 command XFER to enter RAM mode before. For programming BASIC programs to flash memory use command **File → Program flash → CPU fileX** and select file-type "MCS BASIC-52 file". Therefore use the same flash-file where the BASIC interpreter itself is programmed to. Additional setup information is kept in file "Demo2Fpga8032.dat". Content of this file is programmed to flash memory when first BASIC file is flashed, see MCS BASIC-52 interpreter manual for detailed description of it´s content

8.3.2 BASIC demo program source code

Demo BASIC programs (source code) and tokenized ROM code is available on CD, see chapter 9.2

8.4 EAGLE Light

Tool to produce schematics and PCB´s, powerful and easy to use. Can be used to view dlk51 schematic and library or to design user boards for dlk51 and eLAB ...
EAGLE Light, (CadSoft board layout and schematic software limited to non-profit applications or evaluation purposes) available on CD, see chapter 9.2 or **http://www.cadsoft.de**

8.4.1 Schematic dlk51 and library

Schematic and library is available on CD, see chapter 9.2

9 Ressources

For further informations please consult following ressources

9.1 dlk / eLAB link - database

user accessible link database for all themes concerning the ´dlk´ and ´eLAB´ system available at **http://www.seng.de/dlk_database.html** . Including links to: newsgroups, FPGA stuff, Xilinx stuff, software for 8051 / AVR and 8086 CPU´s, VHDL stuff, IP cores, soft-CPU´s, board layout software, tools, support adresses ... If You find something interesting on the web or distribute something via Your own internet area send the link and a short description of the item via eMail to: **info@seng.de** . - Thanks -

9.2 On CD

Pathnames:

D:\AcroRead\WIN9X_NT, Adobe Acrobat Reader

D:\EAGLE, EAGLE Light, CadSoft board layout and schematic

D:\SDCC, SDCC C compiler and documentation

D:\SENG, setup.exe, install- and program-files for "dlk51.exe"

D:\SENG\CPLD\FlashCfgLed, test, on board CPLD, JEDEC file and sources
D:\SENG\CPLD\P017a002, on board CPLD (see chapter 5.10 - remark 5), JEDEC file (see chapter 1.1)
D:\SENG\CPLD\P017a004, on board CPLD (see chapter 5.10 - remark 5), JEDEC file (see chapter 1.1)

D:\SENG\Doc, manual and documentation for dlk51

D:\SENG\EAGLE\dlk51, dlk51 schematic and library

D:\SENG\FPGA\Demo1Fpga8032, FPGA sources
D:\SENG\FPGA\Demo2Fpga8032, FPGA sources
D:\SENG\FPGA\eLABbaseTestA, FPGA sources
D:\SENG\FPGA\eLABbaseTestB, FPGA sources
D:\SENG\FPGA\FlashFastTestLed, FPGA sources
D:\SENG\FPGA\FlashSlowTestLed, FPGA sources
D:\SENG\FPGA\LioTestA, FPGA sources
D:\SENG\FPGA\LioTestB, FPGA sources
D:\SENG\FPGA\Setup, FPGA sources

D:\SENG\MCSbasic52, demo BASIC programs, source code and tokenized ROM code

D:\SENG\SDCC\DemoC8032, extended demo C source code for 8032 CPU
D:\SENG\SDCC\FlashTestLed, simple demo C source code for 8032 CPU
D:\SENG\SDCC\Tools, tools, batches for SDCC

D:\SENG\Source\dlk51, "dlk51.exe" source

where D is the CD drive

Files and updates are also available at "dlk - file area", see **http://www.seng.de/dlk_downloadEnter1_.html** .