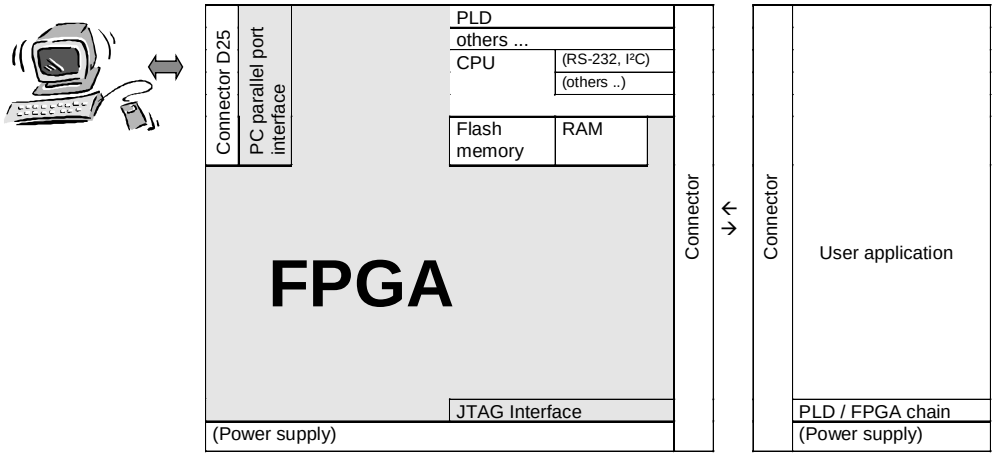
dlk

The ´digital logic kernel´ is an easy to use technology to design, build and program logic blocks containing any kind of CPU with external program memory, programmable logic and flash memory. There is no need for any programming equipment or pre-programming of parts before use. The ´dlk´ is by default a self bootable device. It can be accessed via an integrated PC parallel printer port interface to exchange data or for administration purposes.
The only tool needed to build, program and service devices in the field is a state of the art PC with one parallel printer port. The ´dlk´ is implemented by use of Xilinx parts and design software.
Summary: ´digital logic kernel´= CPU+memory+FPGA+PCinterface = bootable system = ´ease of use´

The ´dlk´concept



Features

- build logic systems by using proven, reliable, expandable and easy to use kernels
- fast development cycles
- adaptable to any kind of CPU with external program memory
- consists of standard FPGA and CPLD parts, no special parts needed
- transfer data to and from those parts via the integrated parallel port interface
- internal bus master can be external PC or internal CPU
- parallel port interface to PC used for data transfer and administration
- parallel port interface reserves minimum amount of internal FPGA, if not used no internal resources are occupied
- administration software included
- software kernel included as DLL
- software and hardware kernel optionally available as source code
- full featured implementation occupies just about 8% the slices of xc2s50 FPGA plus one xc9572xl CPLD
- upgradeable in the field
- build complete logic systems without the need of any kind of programming equipment hardware
- easy expandable design
- compatible to Xilinx ISE WebPACK
- emulation of Xilinx JTAG download cable (DLC5), compatible to iMPACT programming software
- Xilinx ISE WebPACK available for free
- use schematic entry, VHDL, Verilog or ABEL to enter a design

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digital logic kernel - dlk51 *The core of eLABbase*

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What for

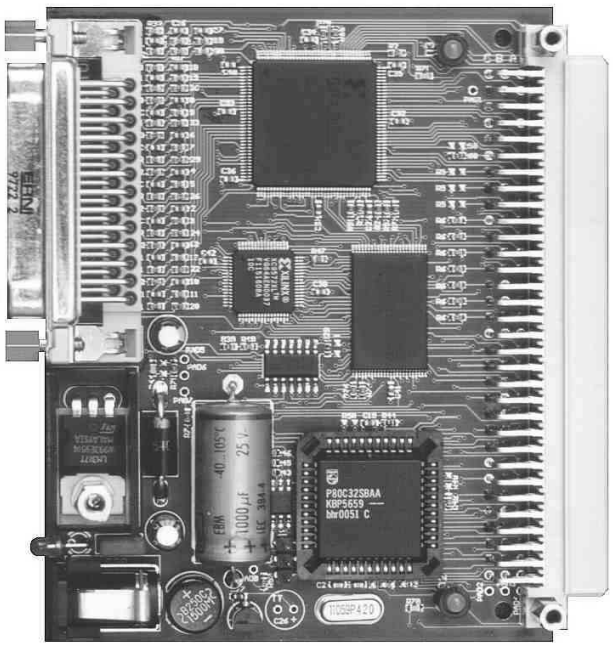
- development platform
- implement logic kernels in any kind of user application
- build standard blocks for re-use in many applications
- rapid prototyping
- for test purposes with need to be accessed by a PC via a standard interface
- as interface between an existing pice of hardware and a PC
- build systems with integrated PC interface
- build systems without expensive development tools
- cross development of controller based hardware on the PC
- for educational use

Implementations

- dlk51, existing
- dlk32, planned, integrating 32-bit (soft-)CPU

dlk51

Hardware



- FPGA xc2s50 (optional xc2s100)
- CPLD xc9572xl
- 8-bit 8032 CPU running at 11MHz0592
- serial RS-232 port connected to CPU
- 16Kbit I²C EEprom connected to CPU
- CPU can be used in bus or I/O mode
- external CPU bus connected to FPGA
- single 512Kx8 flash memory for CPU and FPGA
- two LED´s for debug and display purposes
- ready for LCD display
- reset monitor circuit for power failure detection and external reset
- all 3V3 design
- 2 independent FPGA configuration files in flash memory, selectable via jumper before boottime
- 4 independent 64Kx8 CPU program files in flash memory, selectable via ´dlk51´ software or FPGA setup
- PC or 8032 microcontroller can be used as host CPU for internal bus
- fast data transfer (500Kbytes/sec, typical) to/from PC via PC parallel printer port interface, connector D25 male
- linear power supply on board, input 8-12V DC/12V AC/1500mA (optional 5-12V DC/800mA), connector DIN45323
- all signals available at 96-pin connector DIN 41612
- user extension boards can be installed inline or as stack
- board size 80x100mm
- about 92% of internal xc2s50 FPGA resources (without PC interface 100%) + 32 I/O´s available to user
- Emulation modes for ATMEL AT89isp cable, AVR ISP dongle and XILINX JTAG download cable (DLC5 / Parallel Cable III)
- digital logic kernel for application, test, development and education

digital logic kernel - dlk51 *The core of eLABbase*

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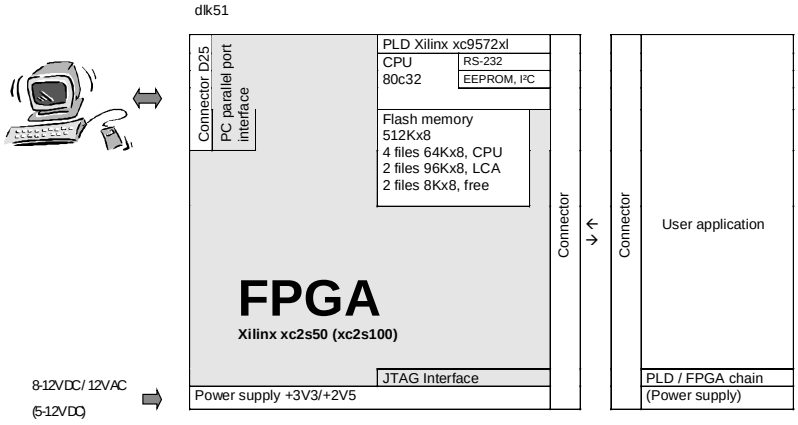
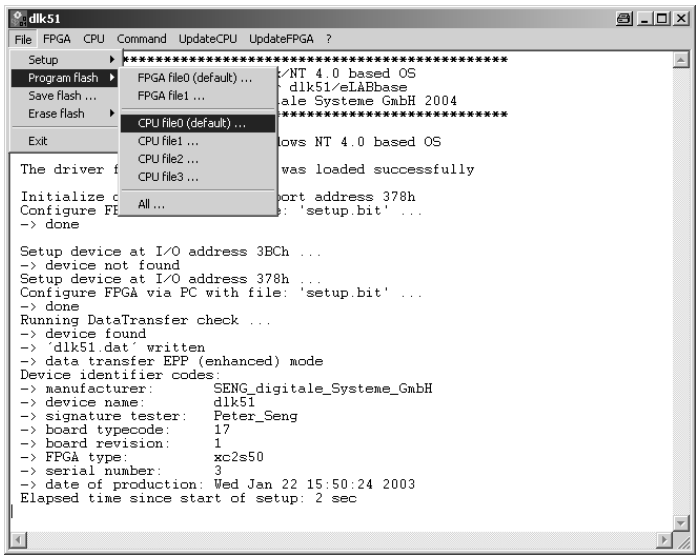


Software



- **Development environment ´dlk51´** for Win9x/NT4.0 based operating systems. Program for system administration of ´dlk51´, including following functions: setup; FPGA-configuration; programming of internal Flash-memory (for CPU and FPGA); integrated command line interpreter (the easy way to include user code); emulation modes for ATMEL AT89isp cable, AVR ISP dongle and XILINX JTAG download cable (DLC5 / Parallel Cable III); support for INTEL MCS BASIC-52 interpreter. Program consists of user interface and a DLL containing all functions. Source code is available, program can be edited and extended by user.
- For programming of ´dlk51´ internal devices (FPGA, CPLD and CPU), powerful **professional tools** are available. Program packages are **available for free via internet**. These products are: XILINX **ISE WebPACK** (integrated software environment for programmable logic devices, simulation and programming tools, schematic entry, VHDL and Verilog compiler), **SDCC C Compiler** (for 8051 CPU´s), INTEL MCS BASIC-52 interpreter (for 8051 CPU´s), **EAGLE light** (board layout and schematic software)

Applications and sources

- See our internet pages (http://www.seng.de/dlk51_.html) for manual, applications, test- and demo-projects as well as **source-code**. From simple AND logic gate to the demanding VHDL projekt (24h real time clock in FPGA / CPLD, control of UART, LCD and several i2c-devices via 8051 ...)
- Link-collection (database) to themes all around ´dlk´, ´eLAB´, FPGA´s, 8051, AVR, VHDL, IP-cores, soft-CPU´s, ... See: (http://www.seng.de/dlk_database.html)

Add-on´s

´dlk51´ is capable of being extended with components of the ´eLAB´ system (http://www.seng.de/eLab_.html) to build a module based all programmable laboratory (for prototyping, testing and training). Modules containing pushbutton switches, LED´s, displays, relais, i2c devices, a CPLD or a microcontroller are members of a growing module family.

User port, connector X2

DIN41612-96 or DIN41651-34+DIN41651-26* (bus connector **or** I/O port connector can be assembled)
peripheral chip select
°CPU signal connected to FPGA
^ RS-232 tranceiver may be installed on board
[2] select FPGA configuration boot file: high or open → file0 (default), low → file1
[3] depending on configuration this pin may be used for JTAG or ISP download cable emulation
[4] see chapter 5.7. Set solder joint for use with eLAB2dlk51-adapter. Default: +UDC not available
[5] depending on CPLD configuration file, not used (default) or charge pump driver (for eLAB2dlk51-adapter), see down

			eLAB base	FPGA Pin		eLAB base	FPGA Pin	
								DIN41651-34
DIN 41612-C	**C**	**B**			**A**			
1	GND	+3V3			GND			**2**
2	(+UDC)[4]	LIO0	P1	102	LIO1	P2	103	**4**
3	+3V3	LIO2	P3	96	LIO3	P4	99	**6**
4	+2V5	LIO4[3]	P5	94	LIO5[3]	P6	95	**8**
5	GND	LIO6[3]	P7	86	LIO7[3]	P8	87	**10**
6	(LTDO) (/RST)	LIO8	P9	84	LIO9	P10	85	**12**
7	(LTDI)	LIO10	P11	80	LIO11	P12	83	**14**
8	(LTMS)	LIO12	P13	75	LIO13	P14	76	**16**
9	(LTCK)	LI0	P31	18	LI1	P32	15	**18**
10	PIO0	LIO14	P15	100	LIO15	P16	101	**20**
11	PIO1	LIO16	P17	93	LIO17	P18	79	**22**
12	PIO2	LIO18	P19	78	LIO19	P20	77	**24**
13	PIO3	LIO20	P21	112	LIO21	P22	113	**26**
14	PIO4[5]	LIO22	P23	114	LIO23	P24	115	**28**
15	PIO5, EnLCD#	LIO24	P25	116	LIO25	P26	117	**30**
16	PIO6, SelFile[2]	LIO26	P27	118	LIO27	P28	121	**32**
17	GND	+3V3			GND			**34**
18	CCI	CCO			LPCLK			
19	CVCC	/EA_VPP			CRST°			
20	A8°	A11°			A14°			
21	A9°	A10°			A12°			**2**
22	/PSEN°	LIO28	P29	123	A13°			**4**
23	ALE°	LIO29	P30	122	A15°			**6**
24	D7°	P3.7_/RD°			P1.7_SDA			**8**
25	D6°	P3.6_/WR°			P1.6_SCL			**10**
26	D5°	P3.5_T1			P1.5			**12**
27	D4°	P3.4_T0			P1.4			**14**
28	D3°	P3.3_INT1			P1.3			**16**
29	D2°	P3.2_/INT0			P1.2			**18**
30	D1°	P3.1_TXD^			P1.1_T2EX			**20**
31	D0°	P3.0_RXD^			P1.0_T2			**22**
32	GND	+3V3			GND			**24**
	A8°	A11°			A14°			**26**
	bus connector*							**DIN41651-26***
		I/O port connector*						

Extent of delivery

- hardware ´dlk51´
- CD-ROM containing software ´dlk51´, manual in PDF format, schematic in EAGLE format, applications including source code for FPGA and 8051
- PC interface cable, D25male/D25female, 1:1
- optional: wall plug-in power supply
- complete ready to use hardware and software package
- fully software programmable up to date hardware solution
- all in one platform for C, VHDL, logic and microcontroller, application and education